REMARKS

Claims 1-16, 41-50, and 66-85 are pending in the current application, and claims 66-67, 80 and 81 are allowed. Claims 1-16, 41-50, 68-79 and 82-85 are rejected. Claims 1, 6-9, 13-14, 41, 43-44, 47-78, 68, 71-76, 78-79, 82, 84-85 have been amended. **If the Examiner does not allow all of the claims after considering this Response, the undersigned requests that the Examiner contact him to schedule and conduct a telephone interview before issuing a subsequent Office Action.**

Examiner Interview

Applicant's Attorney thanks Examiner for the productive Examiner Interview on November 23, 2010 where Examiner indicated that proposed amendments appeared to be allowable. The amendments herein are the same as the proposed amendments presented and discussed in the Interview.

Claim Objection

Claim 1 was objected to because of informalities. Claim 1 is amended. Applicants' Attorney therefore requests withdrawal of this objection.

Rejection Of Claim 1-12, 15-16, 41-46, 49-50, 69-70, 73, 76-77, and 83 Under 35 U.S.C. § 103(a) As Being Unpatentable Over U.S. 7,177,310 to Inagaki In View Of The Examiner's Taking Of Official Notice

Claim 1

Claim 1 as amended recites generating an identifier indicating a processing pipeline without using a virtual address and processing data in response to the identifier without executing a program instruction.

For example, referring, *e.g.*, to FIGS. 4-5 and paragraphs [94] – [102] of the patent application, in an embodiment, a hardwired-pipeline circuit 80 is operable to process data with an indicated processing pipeline 74 without receiving a message indicating the processing pipeline using a virtual address. (see, *e.g.*, paragraph [98]) An input-data handler 120 dissects a message that may have a data payload (*i.e.,* data to be processed by a pipeline 74); a pipeline unit address (*e.g.*, physical address for pipeline unit 78, which comprises pipelines $74_1 – 74_n$); and a pipeline identifier (*e.g.*, an identifier of one of pipelines $74_1 – 74_n$). The data payload is written to a location in DPSRAM 100. A pointer to this location of the data payload and an indication of a destination pipeline (*i.e.,* one of pipelines $74_1 – 74_n$) is stored in an input data queue 112. This pipeline indicator relates to a physical address of a pipeline and not a virtual address. When the selected pipeline is ready to process the data payload, the pointer to the data payload location is sent to the selected pipeline, and the selected pipeline retrieves and processes the data payload.

In contrast, Inagaki does not disclose or suggest generating an identifier indicating a processing pipeline without using a virtual address and processing data in response to the identifier. Referring to FIG. 1 and col. 5, line 66 – col. 6, line 35 of Inagaki, a module 6 includes functional accelerators 11 – 14, which are assigned respective virtual MAC addresses b – e. The module 6 receives an IP packet 134 having a destination IP address 163 (FIG. 3), a unit 105 extracts the destination IP address, and, in response to the extracted IP address, a table 106 provides the virtual MAC address (*e.g.*, address b) of the functional accelerator (*e.g.*, functional accelerator b 11) for processing the data in the IP packet 134. The IP packet 134 (in the form of an Ethernet frame 130) and the virtual MAC address (*e.g.*, address b) are provided to a section 112, which stores the IP packet 134 in the one of the RAMs 150 – 154 (*e.g.*, RAM_b 151) that corresponds to the virtual MAC address (*e.g.*, address b). Subsequently, the module 6 transfers the IP packet 134 from the RAM (*e.g.*, the RAM_b 151) to the one of the function accelerators 11 – 14 (*e.g.*, function accelerator b 11) having the virtual MAC address (*e.g.*, address b) to which the RAM (*e.g.*, the RAM_b 151) corresponds. Consequently, Inagaki's module 6 cannot function as described if it does not use a virtual MAC address to route the IP packet 134 to the appropriate

function accelerator 11 – 14. In fact, per page 3 of the Office Action, Examiner actually agrees that Inagaki uses a virtual address to indicate a pipeline.

Additionally, Applicants' attorney again objects to Examiner's reliance on his Official Notice (*e.g.,* ". . . anything performed in software can be performed solely by hardware and vice-versa") for this and the other rejections in the Office Action as improper because the substance of the Official Notice is conclusion, not fact. Under the Examiner's premise, no apparatus that performs in hardware what was previously performed in software can ever be patentable.

Examiner is reminded that when an Applicant challenges a factual assertion as not properly officially noticed or not properly based upon common knowledge, the Office must support the finding with adequate documentary evidence in the next Office Action if the rejection is to be maintained. (MPEP §2144.03(C)). The present Office Action fails to provide such documentary evidence.

Additionally, proper use of Official Notice requires compliance with several obligations expressly set forth in the *Manual of Patent Examining Procedure*. The Office Action has failed to meet these obligations. Specifically, the Office has failed to satisfy its obligations under *MPEP* § 2144.03. For example, *MPEP § 2144.03 (B)* expressly requires the Office to provide specific factual findings predicated on sound technical and scientific reasoning to support taking Official Notice. The *MPEP* goes on to explain that this means that the Office should present an Applicant with the explicit basis on which Official Notice is based so that the Applicant is able to challenge the assertion in the next reply after the Office action. (*MPEP §2144.03(B)*). Naked assertions about what is allegedly known in the art, like those made at page 5 of the Office Action, cannot satisfy these requirements.

Furthermore, Inagaki fails to disclose or suggest a hardwired pipeline circuit operable without executing a program instruction. For example, referring to Fig. 1 and col. 4, line 67 and col. 5, lines 1-2, Inagaki teaches "a memory 10 for storing . . . a function accelerator_b to a function accelerator_e (11 to 14)." These functional accelerators are, therefore, embodied in software, and, therefore, can only operate by

executing program instructions. Also, Inagaki's claim 11 recites "a found unique address accelerator is implemented by a software."

In response to this latter argument, the examiner states the following on page 4 of the Office Action: "[h]owever, it should be noted that Inagaki makes not a single mention of executing instructions to perform the claimed steps. Hence, it is unclear as to whether Inagaki executes instructions to perform the claimed steps."

First, as discussed above, the examiner is incorrect that "Inagaki makes not a single mention of executing instructions to perform the claimed steps."

But even assuming that the examiner is correct on this point, even the examiner admits that "it is unclear as to whether Inagaki executes instructions to perform the claimed steps." Therefore, Examiner fails to establish a *prima facie* case of obviousness, because even according to the Examiner, it is unclear whether or not Inagaki discloses a hardwired pipeline circuit operable, without executing a program instruction, to process data as recited in claim 1. Furthermore, if Inagaki is unclear as to the claim limitation that the examiner is trying to show, then the Examiner's taking of Official Notice cannot clarify Inagaki.

Claims 2-5

These claims are patentable at least by virtue of their dependencies from claim 1.

Claim 6

Claim 6 as amended recites generating an identifier indicating a destination pipeline without referencing a virtual address and processing data in response to the identifier without executing a program instruction.

In contrast, Inagaki does not disclose or suggest generating an identifier indicating a destination pipeline without referencing a virtual address and processing data in response to the identifier without executing a program instruction. These teaching deficiencies are illustrated in the discussion above relating to claim 1.

Furthermore, the Applicants' attorney objects to the Examiner's taking of Official Notice for the reasons recited above in the discussion above relating to claim 1.

Claim 7

Claim 7 as amended recites generating an identifier indicating a processing pipeline without using a virtual address and processing data in response to the identifier without executing a program instruction.

In contrast, Inagaki does not disclose or suggest generating an identifier indicating a processing pipeline without using a virtual address and processing data in response to the identifier without executing a program instruction. These teaching deficiencies are illustrated in the discussion above relating to claim 1.

Furthermore, the Applicants' attorney objects to the Examiner's taking of Official Notice for the reasons recited above in the discussion above relating to claim 1.

Claims 69-70

These claims are patentable at least by virtue of their dependencies from claim 7.

Claim 8

Claim 8 as amended recites generating an identifier indicating a processing pipeline without referencing a virtual address and processing data in response to the identifier without executing a program instruction.

In contrast, Inagaki does not disclose or suggest generating an identifier indicating a processing pipeline without referencing a virtual address and processing data in response to the identifier without executing a program instruction. These teaching deficiencies are illustrated in the discussion above relating to claim 1.

Furthermore, the Applicants' attorney objects to the Examiner's taking of Official Notice for the reasons recited above in the discussion above relating to claim 1.

Claim 9

Claim 9 as amended recites generating an identifier indicating a destination hardwired pipeline without using a virtual address and processing data in response to the identifier without executing a program instruction.

In contrast, Inagaki does not disclose or suggest generating an identifier indicating a destination hardwired pipeline without using a virtual address and providing the retrieved raw data to the destination hardwired pipeline in response to the identifier without executing a program instruction. In contrast, Inagaki does not disclose or suggest a message specifying a destination hardwired pipeline without using a virtual address. As discussed above in support of the patentability of claim 1, Inagaki's module 6 does not load data into one of the RAMs 150 – 154 (FIG. 1) without first retrieving a virtual MAC address corresponding to a function accelerator 11 – 14 specified for processing the data. Additionally, Inagaki fails to disclose or suggest a hardwired pipeline operable without executing a program instruction to process data. These teaching deficiencies are illustrated in the discussion above relating to claim 1.

Furthermore, the Applicants' attorney objects to the Examiner's taking of Official Notice for the reasons recited above in the discussion above relating to claim 1.

Claims 10-12 and 15-16

These claims are patentable at least by virtue of their dependencies from claim 9.

Claim 41

Claim 41 as amended recites generating an identifier indicating a hardwired pipeline circuit without referencing a virtual address and processing data in response to the identifier without executing a program instruction.

In contrast, Inagaki does not disclose or suggest generating an identifier indicating a hardwired pipeline circuit without referencing a virtual address and processing data in response to the identifier, nor does Inagaki disclose or suggest recited operations without executing a program instruction. These teaching deficiencies are illustrated in the discussion above relating to claim 1.

Claim 42

This claim is patentable at least by virtue of its dependency from claim 41.

Claim 43

Claim 43 as amended recites generating an identifier indicating a hardwired pipeline circuit without using a virtual address and processing data in response to the identifier without executing a program instruction.

In contrast, Inagaki does not disclose or suggest generating an identifier indicating a hardwired pipeline circuit without using a virtual address and processing data in response to the identifier, nor does Inagaki disclose or suggest recited operations without executing a program instruction. These teaching deficiencies are illustrated in the discussions above relating to claim 1.

Claim 83

This claim is patentable at least by virtue of its dependency from claim 43.

Claim 44

Claim 44 as amended recites generating an identifier indicating a hardwired pipeline without referencing a virtual address and processing data in response to the identifier without executing a program instruction.

In contrast, Inagaki does not disclose or suggest generating an identifier indicating a hardwired pipeline without referencing a virtual address and processing data in response to the identifier without executing a program instruction. These teaching deficiencies are illustrated in the discussion above relating to claim 1.

Claims 45-46 and 49-50

These claims are patentable at least by virtue of their dependencies from claim 44.

Claim 73

Claim 73 as amended recites generating an identifier indicating a hardwired pipeline without referencing a virtual address and providing the data to the hardwired pipeline in response to the identifier.

In contrast, Inagaki does not disclose or suggest generating an identifier indicating a hardwired pipeline without referencing a virtual address and providing the data to the hardwired pipeline in response to the identifier. These teaching deficiencies are illustrated in the discussions above relating to claims 1 and 9.

Furthermore, the Applicants' attorney objects to the Examiner's taking of Official Notice for the reasons recited above in the discussion above relating to claim 1.

Claim 76

Claim 76 as amended recites generating an identifier indicating a hardwired pipeline without using a virtual address and providing the data to the hardwired pipeline in response to the identifier.

In contrast, Inagaki does not disclose or suggest generating an identifier indicating a hardwired pipeline without using a virtual address and providing the data to the hardwired pipeline in response to the identifier. These teaching deficiencies are illustrated in the discussions above relating to claims 1 and 9.

Claim 77

This claim is patentable at least by virtue of its dependency from claim 76.

Rejection Of Claims 13-14, 47-48, 68, 71-72, 74-75, 78-79, 82, and 84-85 Under 35 U.S.C. § 103(a) As Being Unpatentable Over Inagaki In View Of The Examiner's Taking Of Official Notice And Further In View Of U.S. 4,914,653 To Bishop

Claim 13

Claim 13 as amended recites generating an identifier specifying a destination hardwired pipeline without referencing a virtual address and providing data to the destination hardwired pipeline in response to the identifier without executing a program instruction.

For example, referring, *e.g.*, to FIGS. 4-5 and paragraphs [94] – [102] of the patent application, in an embodiment, a hardwired-pipeline circuit 80 is operable to process data with an indicated processing pipeline 74 without receiving a message indicating the processing pipeline using a virtual address. (see, *e.g.*, paragraph [98]) An input-data handler 120 dissects a message that may have a data payload (*i.e.,* data to be processed by a pipeline 74); a pipeline unit address (*e.g.*, physical address for pipeline unit 78, which comprises pipelines $74_1 – 74_n$); and a pipeline identifier (*e.g.*, an identifier of one of pipelines $74_1 – 74_n$). The data payload is written to a location in DPSRAM 100. A pointer to this location of the data payload and an indication of a destination pipeline (*i.e.,* one of pipelines $74_1 – 74_n$) is stored in an input data queue 112. This pipeline indicator relates to a physical address of a pipeline and not a virtual address. When the selected pipeline is ready to process the data payload, the pointer to the data payload location is sent to the selected pipeline, and the selected pipeline retrieves and processes the data payload.

In contrast, Inagaki and Bishop, either alone or combined, do not disclose or suggest generating an identifier specifying a destination hardwired pipeline without referencing a virtual address and providing data to the destination hardwired pipeline in response to the identifier without executing a program instruction. Referring to FIG. 1 and col. 5, line 66 – col. 6, line 35 of Inagaki, a module 6 includes functional accelerators 11 – 14, which are assigned respective virtual MAC addresses b – e. The module 6 receives an IP packet 134 having a destination IP address 163 (FIG. 3), a unit

105 extracts the destination IP address, and, in response to the extracted IP address, a table 106 provides the virtual MAC address (*e.g.*, address b) of the functional accelerator (*e.g.*, functional accelerator b 11) for processing the data in the IP packet 134. The IP packet 134 (in the form of an Ethernet frame 130) and the virtual MAC address (*e.g.*, address b) are provided to a section 112, which stores the IP packet 134 in the one of the RAMs 150 – 154 (*e.g.*, RAM_b 151) that corresponds to the virtual MAC address (*e.g.*, address b). Subsequently, the module 6 transfers the IP packet 134 from the RAM (*e.g.*, the RAM_b 151) to the one of the function accelerators 11 – 14 (*e.g.*, function accelerator b 11) having the virtual MAC address (*e.g.*, address b) to which the RAM (*e.g.*, the RAM_b 151) corresponds. Consequently, Inagaki's module 6 cannot function as described if it does not use a virtual MAC address to route the IP packet 134 to the appropriate function accelerator 11 – 14. In fact, per page 3 of the Office Action, Examiner actually agrees that Inagaki uses a virtual address to indicate a pipeline.

Additionally, Inagaki and Bishop, either alone or combined, fails to disclose or suggest a hardwired-pipeline circuit comprising the recited components operable without executing a program instruction. This teaching deficiency is illustrated in the discussion above relating to claim 1.

Bishop and the Examiner's Official Notice fail to remedy these teaching deficiencies. Consequently, the combination of Inagaki, the Examiner's Official Notice, and Bishop does not render claim 13 obvious.

Furthermore, the Applicants' attorney objects to the Examiner's taking of Official Notice for the reasons recited above in the discussion above relating to claim 1.

Claim 14

Claim 14 as amended recites generating an identifier specifying a destination hardwired pipeline without using a virtual address and providing data to the destination hardwired pipeline in response to the identifier, and recites a hardwired pipeline operable without executing a program instruction.

In contrast, the combination of Inagaki, the Examiner's Official Notice, and Bishop does not disclose or suggest generating an identifier specifying a destination

hardwired pipeline without using a virtual address and providing data to the destination hardwired pipeline in response to the identifier, nor does the combination of Inagaki, the Examiner's Official Notice, and Bishop disclose or suggest a hardwired pipeline operable to process data without executing a program instruction. These teaching deficiencies are illustrated in the discussion above relating to claim 1 and Bishop fails to remedy this teaching deficiency.

Claim 47

Claim 47 as amended recites generating an identifier indicating a hardwired pipeline without using a virtual address and processing data in response to the identifier without executing a program instruction.

In contrast, the combination of Inagaki, the Examiner's Official Notice, and Bishop does not disclose or suggest generating an identifier indicating a hardwired pipeline without using a virtual address and processing data in response to the identifier, nor does the combination of Inagaki, the Examiner's Official Notice, and Bishop disclose or suggest performing operations without executing a program instruction. This teaching deficiency is illustrated in the discussion above relating to claim 1 and Bishop fails to remedy this teaching deficiency.

Claim 48

Claim 48 as amended recites generating an identifier indicating a hardwired pipeline without referencing a virtual address and processing data in response to the identifier.

In contrast, the combination of Inagaki, the Examiner's Official Notice, and Bishop does not disclose or suggest generating an identifier indicating a hardwired pipeline without referencing a virtual address and processing data in response to the identifier, nor does the Examiner's Official Notice, and Bishop disclose or suggest processing data with a hardwire pipeline without executing a program instruction. This teaching deficiency is illustrated in the discussion above relating to claim 1 and Bishop fails to remedy this teaching deficiency.

Claim 68

Claim 68 as amended recites generating an identifier indicating a pipeline without using a virtual address and processing data in response to the identifier.

In contrast, the combination of Inagaki, the Examiner's Official Notice, and Bishop does not disclose or suggest generating an identifier indicating a pipeline without using a virtual address and processing data in response to the identifier, nor does the combination of Inagaki, the Examiner's Official Notice, and Bishop disclose or suggest a hardwired pipeline circuit operable to perform operations without executing a program instruction. This teaching deficiency of Inagaki and the Examiner's Official Notice is illustrated in the discussion above relating to claim 1, and Bishop fails to remedy this teaching deficiency.

Furthermore, the Applicants' attorney objects to the Examiner's taking of Official Notice for the reasons recited above in the discussion above relating to claim 1.

Claim 71

Claim 71 as amended recites generating an identifier indicating a processing pipeline without referencing a virtual address and processing data in response to the identifier.

In contrast, the combination of Inagaki, the Examiner's Official Notice, and Bishop does not disclose or suggest generating an identifier indicating a processing pipeline without referencing a virtual address and processing data in response to the identifier.

These teaching deficiencies of Inagaki and the Examiner's Official Notice are illustrated in the discussions above relating to claim 7; and Bishop fails to remedy these teaching deficiencies.

Furthermore, the Applicants' attorney objects to the Examiner's taking of Official Notice for the reasons recited above in the discussion above relating to claim 1.

Claim 72

Claim 72 as amended recites generating an identifier indicating a processing pipeline without using a virtual address and processing data in response to the identifier.

In contrast, the combination of Inagaki, the Examiner's Official Notice, and Bishop does not disclose or suggest generating an identifier indicating a processing pipeline without using a virtual address and processing data in response to the identifier.

These teaching deficiencies of Inagaki and the Examiner's Official Notice are illustrated in the discussions above relating to claims 1 and 7; and Bishop fails to remedy these teaching deficiencies.

Furthermore, the Applicants' attorney objects to the Examiner's taking of Official Notice for the reasons recited above in the discussion above relating to claim 1.

Claim 74

Claim 74 as amended recites generating an identifier indicating a processing hardwired pipeline without using a virtual address and providing the data to the hardwired pipeline response to the identifier, and recites a hardwired pipeline operable to process data without executing a program instruction.

In contrast, the combination of Inagaki, the Examiner's Official Notice, and Bishop does not disclose or suggest generating an identifier indicating a processing hardwired pipeline without using a virtual address and providing the data to the hardwired pipeline response to the identifier, nor does this combination disclose or suggest a hardwired pipeline operable to process data without executing a program instruction.

These teaching deficiencies of Inagaki and the Examiner's Official Notice are illustrated in the discussion above relating to claim 1; and Bishop fails to remedy these teaching deficiencies.

Claim 75

Claim 75 as amended recites generating an identifier indicating a processing hardwired pipeline without referencing a virtual address and providing the data to the hardwired pipeline response to the identifier and recites a hardwired pipeline circuit operable to perform actions without executing a program instruction.

In contrast, the combination of Inagaki, the Examiner's Official Notice, and Bishop does not disclose or suggest generating an identifier indicating a processing hardwired pipeline without referencing a virtual address and providing the data to the hardwired pipeline response to the identifier, nor does this combination disclose or suggest a hardwired pipeline circuit operable to perform actions without executing a program instruction.

These teaching deficiencies of Inagaki and the Examiner's Official Notice are illustrated in the discussion above relating to claim 1; and Bishop fails to remedy these teaching deficiencies.

Claim 78

Claim 78 as amended recites generating an identifier indicating a processing hardwired pipeline without referencing a virtual address and providing the data to the hardwired pipeline response to the identifier, and recites a hardwired pipeline circuit operable to perform actions without executing a program instruction.

In contrast, the combination of Inagaki, the Examiner's Official Notice, and Bishop does not disclose or suggest generating an identifier indicating a processing hardwired pipeline without referencing a virtual address and providing the data to the hardwired pipeline response to the identifier, nor does this combination disclose or suggest a hardwired pipeline circuit operable to perform the recited actions without executing a program instruction.

These teaching deficiencies of Inagaki and the Examiner's Official Notice are illustrated in the discussion above relating to claim 1; and Bishop fails to remedy these teaching deficiencies.

Claim 79

Claim 79 as amended recites generating an identifier indicating a processing hardwired pipeline without using a virtual address and providing the data to the hardwired pipeline response to the identifier, and recites a hardwired pipeline circuit operable to perform actions without executing a program instruction.

In contrast, the combination of Inagaki, the Examiner's Official Notice, and Bishop does not disclose or suggest generating an identifier indicating a processing hardwired pipeline without using a virtual address and providing the data to the hardwired pipeline response to the identifier, nor does this combination disclose or suggest a hardwired pipeline circuit operable to perform the recited actions without executing a program instruction.

These teaching deficiencies of Inagaki and the Examiner's Official Notice are illustrated in the discussion above relating to claim 1; and Bishop fails to remedy these teaching deficiencies.

Claim 82

Claim 82 as amended recites generating an identifier indicating a processing hardwired pipeline circuit without referencing a virtual address and processing data response to the identifier, and recites a method involving a hardwired pipeline circuit that includes steps which occur without executing a program instruction. For example, processing data with a hardwired pipeline circuit and loading the processed data into a memory.

In contrast, Inagaki, the Examiner's Official Notice, and Bishop does not disclose or suggest operation without executing a program instruction or generating an identifier indicating a processing hardwired pipeline circuit without referencing a virtual address and processing data response to the identifier. These teaching deficiencies of Inagaki and the Examiner's Official Notice is illustrated in the discussion above relating to claim 1; and Bishop fails to remedy this teaching deficiency.

Claim 84

Claim 84 as amended recites generating an identifier indicating a processing hardwired pipeline circuit without using a virtual address and processing data response to the identifier without executing a program instruction.

In contrast, Inagaki, the Examiner's Official Notice, and Bishop does not disclose or suggest generating an identifier indicating a processing hardwired pipeline circuit without using a virtual address, nor does Inagaki, the Examiner's Official Notice, and Bishop disclose or suggest processing data with a hardwired pipeline circuit without executing a program instruction.

These teaching deficiencies of Inagaki and the Examiner's Official Notice are illustrated in the discussions above relating to claim 1; and Bishop fails to remedy these teaching deficiencies.

Claim 85

Claim 85 as amended recites generating an identifier indicating a processing hardwired pipeline circuit without referencing a virtual address and processing data response to the identifier without executing a program instruction.

In contrast, Inagaki, the Examiner's Official Notice, and Bishop does not disclose or suggest generating an identifier indicating a processing hardwired pipeline circuit without referencing a virtual address, nor does Inagaki, the Examiner's Official Notice, and Bishop disclose or suggest processing data with a hardwired pipeline circuit without executing a program instruction.

These teaching deficiencies of Inagaki and the Examiner's Official Notice are illustrated in the discussions above relating to claim 1; and Bishop fails to remedy these teaching deficiencies.

Conclusion

In view of the foregoing, the application is believed to be in a condition for allowance. The Examiner is encouraged to contact the undersigned via telephone if a conference would expedite prosecution of this matter.

The filing of this document constitutes a request for any needed extension of time. The Commissioner is hereby authorized to charge any deficiency of fees submitted herewith, or credit any overpayment, to Deposit Account No. 07-1897.

Dated the 15th day of December, 2010

Respectfully submitted,

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